THAT WHICH IS CLAIMED IS:

1. A solid state imaging device comprising a two-dimensional array of pixels forming an image plane, and readout electronics for reading out signals from the pixels in a predetermined manner; and in which the readout electronics are located off said image plane.

2. The device of claim 1, in which each pixel is connected to its associated readout electronics via a multiconductor signal bus.

3. The device of Claim 2, in which each pixel comprises a photosensitive diode and switching means for resetting and discharging the diode; and in which the switching means consists only of a first transistor for applying a reset pulse and a second transistor operable to connect the diode to a predetermined conductor of said multi-conductor signal bus.

4. The device of Claim 2 or Claim 3, in which the signal bus conductors are stacked.

5. The device of any preceding Claim, in which the readout electronics are located at one side of the array.

6. The device of any one of Claims 1 to 5, in which the readout electronics are located on two opposite sides of the array.

7. The device of any preceding Claim, in which all pixels in the array are reset simultaneously and are read out simultaneously.

8. The device of any preceding Claim, in which the readout electronics comprises, for each pixel, a first store for a reset value and a second store for a read out value; and the readout electronics is effective to modify the read out value of a given pixel by the stored reset value for that pixel.

9. The device of Claim 8, in which the readout electronics further includes, for each pixel, a further store for a second reset value whereby the current reset and read out values may be processed simultaneously with applying a new reset pulse.

10. The device of Claim 9, in which the readout electronics further includes a differential amplifier connectable to said stores, and means for putting the amplifier into a common mode reset state prior to reading out a signal.